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Application of the Plasma Etching technique to Fabricating a Concave-type Pt Electrode Capacitor

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We have used a plasma etching method in order to develop a concave-type Pt electrode capacitor to overcome the limitation of conventional stack-type capacitor in a small critical-dimension (CD) pattern. We have deposited Pt layer on the concave-type structure made by patterning of SiO_2 and subsequently we separated the adjacent nodes by etch-back process with photoresist (PR) as a protecting layer.

Keywords : *Pt, Etching, concave, CD.*

1. Introduction

In order to increase the storage capacity per cell for 4 Giga-bit dynamic random access memory (DRAM) and beyond, the usage of barium strontium titanate (BST) capacitor has been considered. As an electrode material for BST capacitor, various materials such as platinum (Pt), iridium (Ir), ruthenium (Ru), and ruthenium oxide (RuO_2) have been studied. Among them, Pt is most appropriate because of its good oxidation-resistance, high electrical conductivity, and low leakage current characteristics.[1),2)]

In order to use the Pt as an electrode material in the stacked capacitor cell structure successfully, Pt etching technique, in order to pattern the bottom electrode, has been developed.[3)-5)] However, as Pt has a low reactivity and its etching products have low vapor pressures,[6),7)] the etching of Pt proceeds by physical sputtering. Accordingly, Pt has a low etch slope and thus, as the adjacent nodes are connected with Pt, the bottom Pt storage nodes cannot be separated from their adjacent storage nodes especially in a very low critical dimension (CD) pattern.[8)-11)]

In order to allow for lateral shrinkage of the cell sizes while keeping the required cell capacitance without employing the difficult Pt electrode etching, we have developed a concave-type cell structure,[12)] revealing that the above method is suitable for the storage node pattern in the CD of 0.17 μm and below.

2. Experimental

The fabrication sequence of concave-type Pt/BST/Pt capacitor is shown in Fig. 1. After forming a concave structure with SiO_2, the bottom electrode Pt layer is deposited. The protective photoresist (PR) layer is deposited, and then the etch back is performed to isolate the Pt layer of each concave structure. After removing the remained PR by ashing, BST and the top electrode Pt layer are deposited to form a capacitor.

The schematic of a reactive ion etcher (RIE) used in this work is shown in our previous work.[12)] The combination of high-radio-frequency power (HRF), 13.56 MHz and low-radio frequency power (LRF), 450 kHz, in addition to the low operating pressure (<10 mTorr) results in high-energy ion bombardment. The SiO_2 etching was performed to make a concave structure and a mixture of Ar, CF_4, and CHF_3 gas was used as an etchant. In the Pt etchback process, the Ar gas and Cl_2 gas were employed as an etchant. In the photoresist etchback process, the O_2 gas was used as an etchant.

3. Results and discussion

We have fabricated the etching profile of the concave structure in a pattern with a CD of 0.17 μm, using the $Ar/CF_4/CHF_3$ plasma (not shown here). The SiO_2 to PR etch selectivity increases by increasing CHF_3 gas flow rate, regardless of HRF power and pressure. The SiO_2 to PR etch selectivity increases by increasing HRF power, regardless of the CHF_3 gas flow rate and pressure. Since the high SiO_2 to PR etch selectivity is crucial for obtaining a vertical profile with a high aspect ratio, we have used an etching condition with a HRF power of 700 W, a LRF power of 0 W, a CHF_3 flow rate of 90 sccm, and a pressure of 70 mTorr, resulting in the SiO_2 to PR etch selectivity

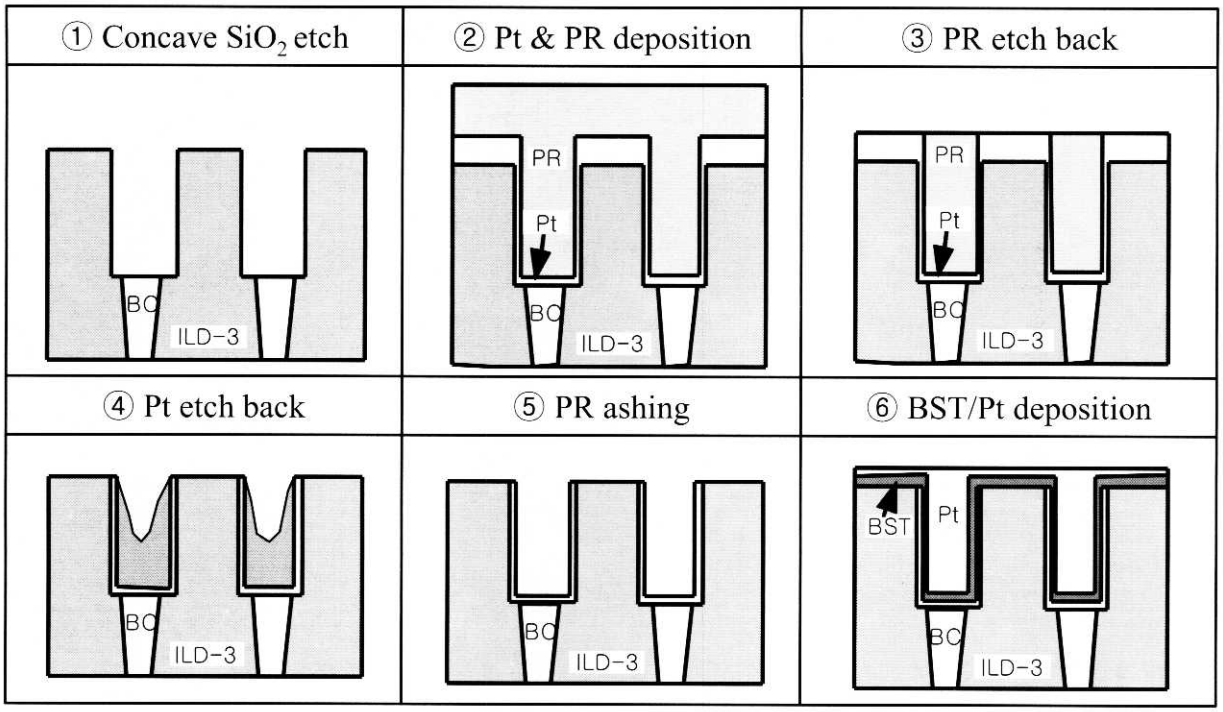


Fig. 1. The fabrication sequence of concave-type Pt/BST/Pt capacitor (ILD-3 represents the interlayer dielectrics of SiO_2 and "BC" represents the buried contact).

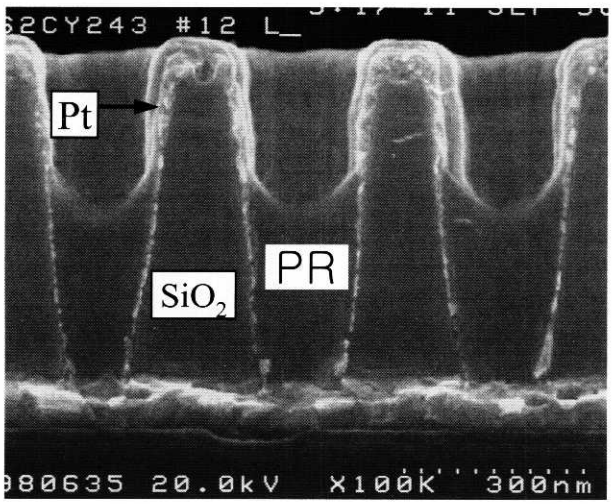


Fig. 2. Concave-type structure (a) before and (b) after the etchback of photoresist (PR) layer.

of 2.4. In order to evaluate the effect of LRF power, we have changed the LRF power from 0 W to 200 W, with an HRF power of 700 W and a pressure of 70 mTorr. The SiO_2 to PR etch selectivity decreases by increasing the LRF power from 0 W to 200 W.

After forming the concave-type structure by etching SiO_2 layer, we deposit the Pt layer which is used as the bottom electrode of capacitor. On top of it, we coat the PR layer to protect the underlying Pt layer. Since only the Pt layer inside the hole of the concave structure is utilized as the bottom electrode, the coated PR layer and subsequently Pt layer outside the hole needs to be removed. For our etchback process, the chamber pressure was 30 mTorr and the O_2 gas flow rate was 50 sccm, with the HRF (13.56 MHz) power and the LRF (450 kHz) power of 600 W and 0 W, respectively. The resulting PR etch rate and etch uniformity are about 6200 Å/min and less than 5 %, respectively. Fig. 2 shows the profiles of the concave-type structure after the etchback of PR layer. We reveal that the Pt layer outside the concave hole is slightly exposed after the etchback process and the Pt layer is not eroded due to the sufficiently high (~ 30 mTorr) etching pressure and resulting low Pt etch rate.

The height of the remaining PR inside the concave hole should be optimized. If the height is too high, some concave holes will have an unwanted PR layer on top of the Pt layer outside the hole. If the height is too low, the PR layer protecting the bottom Pt electrode may be completely eroded during the following Pt etchback process and the bottom Pt layer will be damaged.

In order to separate the Pt layer inside each concave hole and to form a bottom electrode, we remove the Pt layer deposited outside the concave hole by etchback

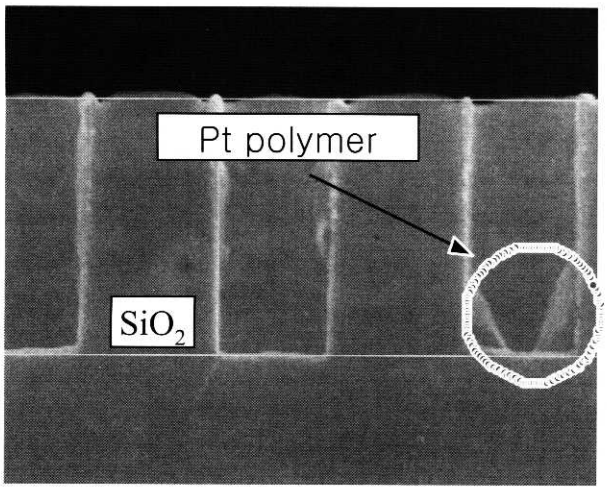


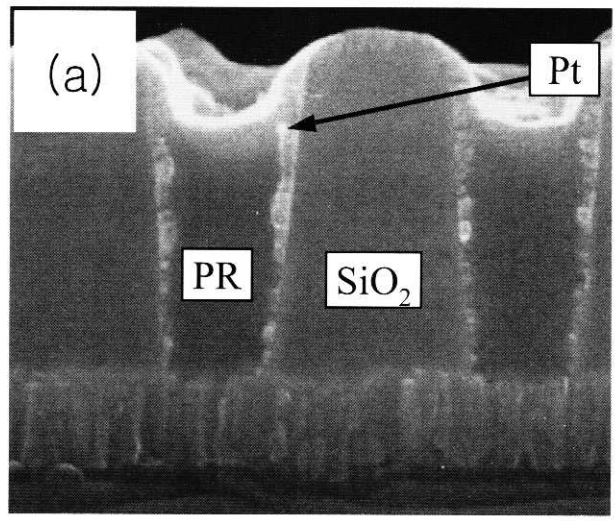
Fig. 3. Pt polymer is generated on the bottom of the hole by the excessive etching of Pt.

process. We etched the Pt, PR, and SiO_2 layer concurrently and etched up to the point where the height of the etched SiO_2 layer is about 80 % of the original height.

In our experimet, we observe the air pockets inside the PR in the concave hole. The presence of air pockets will promote the erosion of PR and thus, the bottom Pt layer inside the hole will be exposed. Fig. 3 shows that the Pt polymer is generated on the bottom of the hole by the unwanted etching of the Pt. Since this generated Pt polymer cannot be removed during the following ashing and strip process and thus, disable the bottom Pt electrode, we suggest that the PR layer should be deposited without generating the air pockets inside. Since the generation of the air pocket is related to high revolution speed of PR coater, we are developing a technique to use low-viscosity photoresist without sacrificing the deposition uniformity.

In this step, the Pt to PR etch selectivity needs to be sufficiently high, otherwise the PR layer inside the hole will be eroded away. Fig. 4 shows the change of the profiles depending on the etchback condition with varying process variables. The etching pressure is set to 5 mTorr, because the Pt is mainly etched by physical sputtering and thus, the high pressure reduces the Pt etch rate. When the LRF power is 0 W and the Ar and Cl_2 gas flow rates are 20 sccm and 5 sccm, respectively, the Pt to PR etch selectivity is 1.9 (Fig. 4 (a)). However, if the Pt to PR etch selectivity is relatively low (Fig. 4 (b)), the excessive erosion of PR inside the concave hole is observed.

After the Pt layer outside the concave hole is removed and thus, the bottom electrodes are separated, we add an overetch step in considering the etch uniformity. Fig. 5 (a) shows ths profile after the just-etch process. Fig. 5



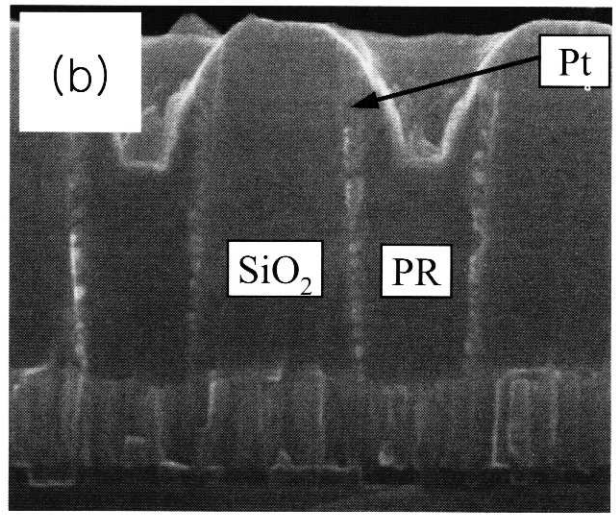
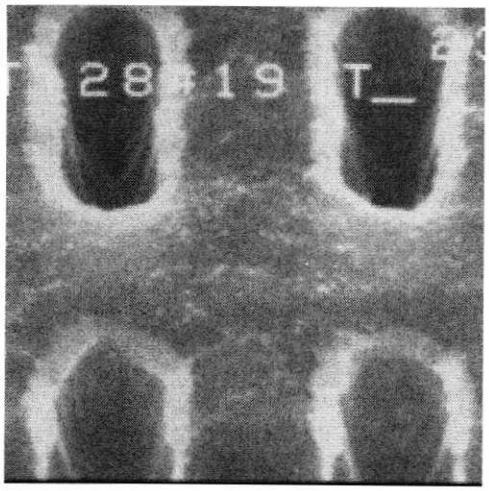
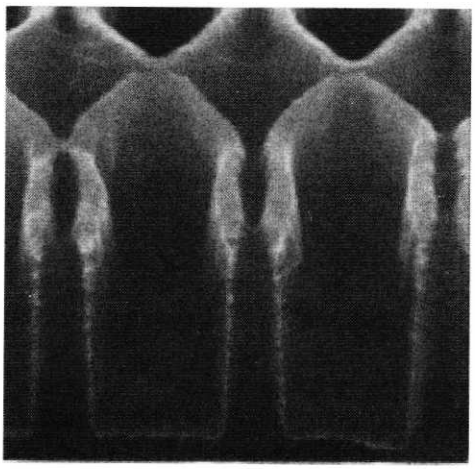


Fig. 4. Change of the profiles depending on the etchback condition. (a) The Pt to PR etch selectivity is about 1.9. (b) The Pt to PR etch selectivity is low.

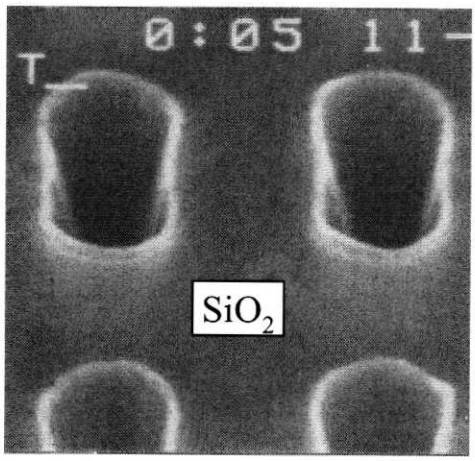
(b) shows the profile using an overetch step of the same recipe as the mainetch step, revealing that the SiO_2 between the nodes are excessively etched. Therefore, we have used an overetch step with HRF power and LRF power of 600 W and 100 W, with a pressure of 30 mTorr, and with Ar and Cl_2 flow rates of 20 sccm and 10 sccm, respectively. In this overetch process, the etch rates of Pt, SiO_2, and PR are about 1000 Å/min, irrespective of etching material. Fig. 5 (c) reveals the SiO_2 between the nodes are not eroded excessively, and the surface of SiO2 is relatively smooth. After completing the Pt etchback process, we remove the remaining PR inside the concave



(a)



(b)



(c)

Fig. 5. Change of the profiles depending on the overetch condition. (a) After just-etch process. (b) After the overetch process with a SiO_2 to Pt etch selectivity of less than 1. (c) After the overetch process with a SiO_2 to Pt etch selectivity of about 1.

hole, and subsequently deposit the BST layer and the top electrode Pt layer, forming the capacitor structure.

4. Conclusions

We suggest to introduce a concave-type storage node pattern and study on issues relevant to the etching technique. In order to form a concave structure with SiO_2, we have tried to elevate the SiO_2 to PR etch selectivity. We deposit the protective PR layer and then the etch back is performed to isolate the Pt layer of each concave structure. The height of the remaining PR inside the concave hole is optimized. The relative etch rates of Pt, PR, and SiO_2 are optimized in the Pt etchback process.

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