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Effects of Current Wave Forms and Current Densities on the Electroplated Cu Interconnection in Damascene Plating

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Effects of three different types of current waveforms and current densities on damascene copper line filling capability were investigated. The electroplating solution developed for printed circuit board (PCB) was used for Damascene plating. Three different types of current wave forms i.e. direct current (DC), Pulsed current, and periodic (PR) current methods were chosen for electroplating with the variation of current densities. The cross-section profiles of deposited wafers were analyzed by Field Emission Scanning Electron Microscope (FE-SEM). Trenches were successfully superfilled without void for Cu lines with 0.4 and 0.8㎛ width according to each current waveform. Each current waveform was optimized with the proper current density values. The critical causes for the center and the sidewall void formations were investigated. Copper plating profiles due to DC current waveform showed center void in the final stage of plating because the copper deposition on the trench top corner was faster than those inside of trench. On the contrary, Pulsed or PR current methods tend to result in center voids due to the faster deposition on the sidewall. Sidewall void formation could be attributed to the localized corrosion of copper seed layers due to long immersion of the wafer in the electrolyte at zero current state before plating.

Keywords : Copper, Superfilling, Damascene plating, Current wave form, Current density

1. Introduction

Ever since the development of the integrated circuit about 40years ago, the most pervasively used materials for the fabrication of the wiring structure have been Al as the conductor. As interconnect continue to scale down, the relatively high resistivity of Al became the major problems. The problems are RC delay time and low resistance of elecrtromigration and stressmigration.[1-2] Therefore new material is required as the substitute for Al.

Cu provides desirable high conductivity, 1.67Ωcm, compared with 3.0(cm of Al. For that reason Cu has advantage of the short RC delay time over Al.[1,5] Since the allowed current density of Cu can be more improved due to the higher conductivity and electromigration resistance than Al, the interconnect scale can be reduced. Different from to the conventional Al interconnection by subtractive metal etching of a planer Al film, Cu interconnect is introduced by trenches etched in the dielectric that are subsequently filled with metal.[3] This process is called Damascene process. It is getting difficult to fill trench as the trench width becomes smaller and the aspect ratio bigger. Therefore various deposition methods have been evaluated for copper including PVD, CVD, electroless plating and electroplating. PVD method tends to form center void because of poor step coverage while CVD method may form seam because of conformal deposition. However, in case that Cu electroplating onto the inside trenches can occur preferentially at the bottom, void free deposition can be obtained. This special phenomenon is called superfilling, also known as bottom-up.[1] Filling in trench by electroplating method depends on various parameters such as agitation, additives, current waveforms and current densities.[4] For the damascene process, the trench geometry results in a lower flux of the inhibitor to the bottom of the feature than to the external surface. Consequently, the metal deposition kinetics proceeds more rapidly at the bottom of the trench than at sidewall of the trench, which results in superfilling. Current density and types of wave forms has an effect on the microstructure of Cu film.[4] DC (direct current), Pulse (pulse

current), PR (periodic current) waveforms are typically used for Cu electroplating. DC method may offer the economical cost for filling in trench, but it can disturb ideal damascene process due to the current crowding phenomenon occurred at the trench corner. On the contrary, Pulse or PR methods can avoid current crowding phenomenon, because of the repetition of the on and off time[5] and the better throwing power due to the higher current density, respectively.[6]

Therefore the optimal combination of additives, current waveform, and current density should be chosen for the submicron trench filling without void.

In this present work, the relationship between types of current waveforms and current densities among parameters was focused on and the causes of the center and the sidewall void formation were also investigated.

2. Experimental

Cu electroplating was performed on 0.25㎛ (aspect ratio 4:1), 0.4㎛ (aspect ratio 2.5:1) and 0.8㎛(aspect ratio 1.25 :1) width trench-pattern silicon substrate. To begin with TaN films as diffusion barriers and Cu films as seedlayers had been deposited by ionized metal plasma PVD. The wafers were cleaned with acetone for removing an organic compound and with dilute sulfuric acid for removing an oxide film on Cu seedlayer respectively. After cleaning process, the wafers were held on the wafer holder for plating. The copper electroplating solution used in this experiment consisted of $CuSO_4.5H_2O$, HCl and some additives. During Cu electroplating, the solution temperature was maintained at 25℃. Three different types of current wave forms such as DC, Pulse and PR were used in this work. Frequency was kept at 50Hz for Pulse and PR electroplating. On and off time cycle of Pulse plating was kept at 1 : 1 and forward and reverse current cycle of PR plating was 2 : 1. The cathodic current densities for each current wave form were 1, 3, 7 A/dm². Electroplating equipment used in this work was fabricated by Sungwonforming Inc, Seoul, Korea. Cathode and anode electrodes were located at the top and the bottom of electroplating cell and fountain method was used for agitation. The pretreated wafer with Cu seedlayer and Cu electrode containing phosphorous were used as cathode and anode, respectively. The wafer was dipped into plating bath for a while before electroplating, in order that the wafer surface should be wet uniformily with the electrolyte. Deposited wafer was cleaned with distilled water and dried with nitrogen gas. The cross-section image of deposited wafers were analyzed by FE-SEM (field emission scanning electron microscope).

3. Results and Discussion

The wafers were electroplated by three different types of current wave forms, i.e. DC, Pulse and PR plating methods with various current densities of 1, 3, 7 A/dm². Figure 2, 3, 4 are the FE-SEM cross-section images of the electroplated 0.25, 0.4 and 0.8㎛ trenches. The trenches were electroplated by Pulse (Figure 2), DC (Figure 3) and PR (Figure 4) plating methods. For all 0.25 ㎛ trenches electroplated by Pulse, DC and PR and at current densities of 1, 3, 7 A/dm², void defects occurred. However, 0.4 and 0.8㎛ trenches were electroplated by Pulse plating method at 1, 3, 7 A/dm² did not show any voids. For DC plating method, trenches electroplated at 3, 7 A/dm² did not have any voids, but 0.4㎛ trench at 1A/dm² had voids. Trenches electroplated by PR plating did not show voids at 3A/dm² only. The trenches wider than 0.4㎛ were successfully filled without any void, irrespective of type of plating methods. Current density values were optimized depending on types of wave forms. The reason is that electroplating velocity was different at each part of trench, dependant on current waveforms. Two kinds of voids were observed. One is the center void and the other is the sidewall void. Half-filled trenches were examined by FE-SEM in order to clarify the cause of center void formation(Figure 5). Electroplating rates at the bottom, the side and the top parts of the trench were compared each other. Figure 6. shows the ratio of the bottom growth rate to the side growth rate with increasing trench width.

As shown in figure 6(a), for DC plating, the growth rate on top of the trench is faster than those in Pulse and in PR plating. This indicates that the growth rate at edges of the trench is faster than that on the bottom sites. Consequently, the closure of the entrance occurs before the trench is filled completely with Cu, resulting in a center void in side of the trench. This is due to the current densities concentrated at the entrance part of trench.

On the other hand, the reason why the growth rate on top part is slower for Pulse and PR plating is due to the

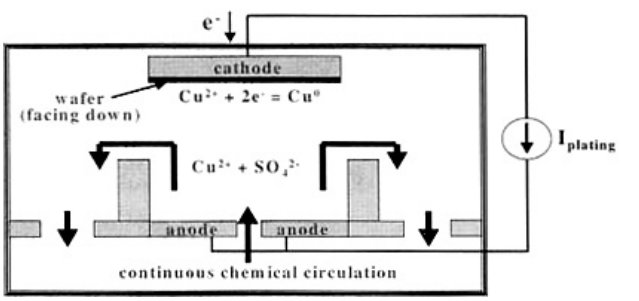
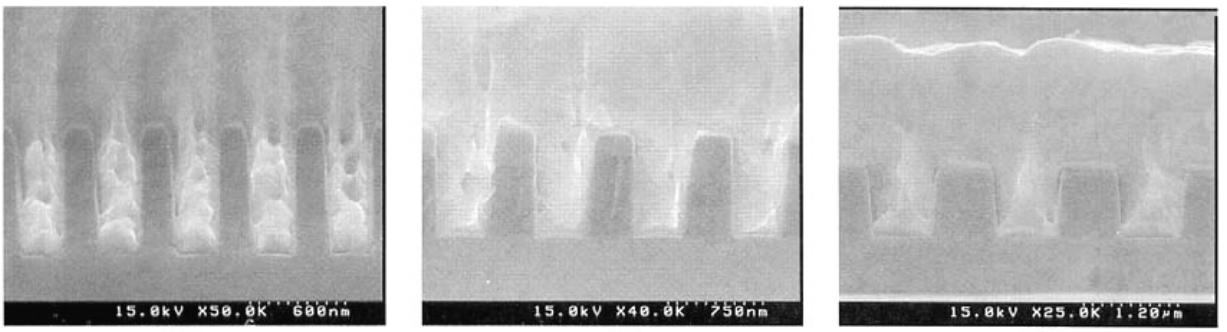


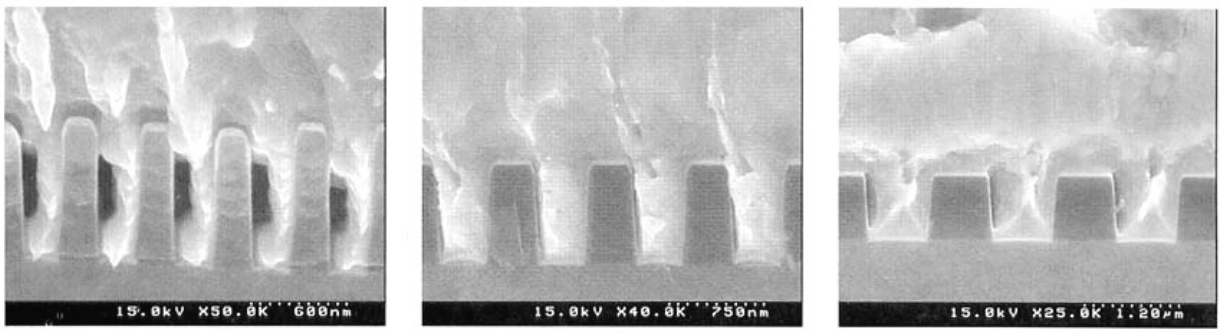
Fig. 1. Schematic drawing of Cu electroplating equipment.

(a) $1A/dm^2$



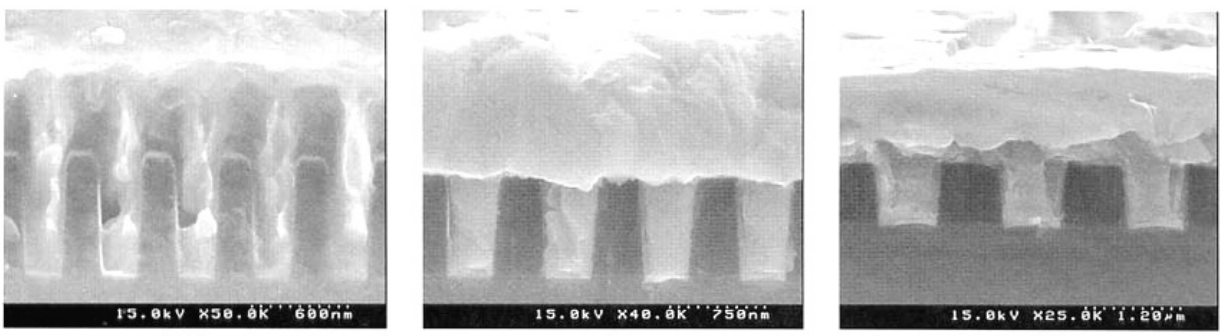
0.25μm 0.4μm 0.8μm

(b) $3A/dm^2$



0.25μm 0.4μm 0.8μm

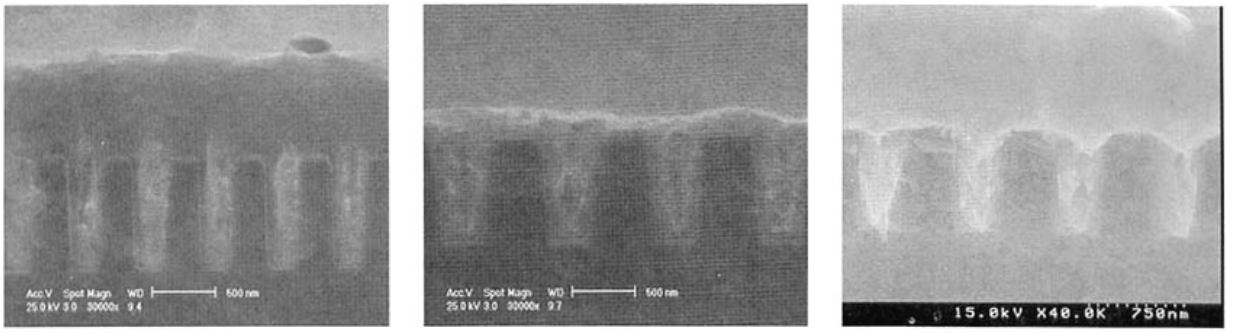
(c) $7A/dm^2$



0.25μm 0.4μm 0.8μm

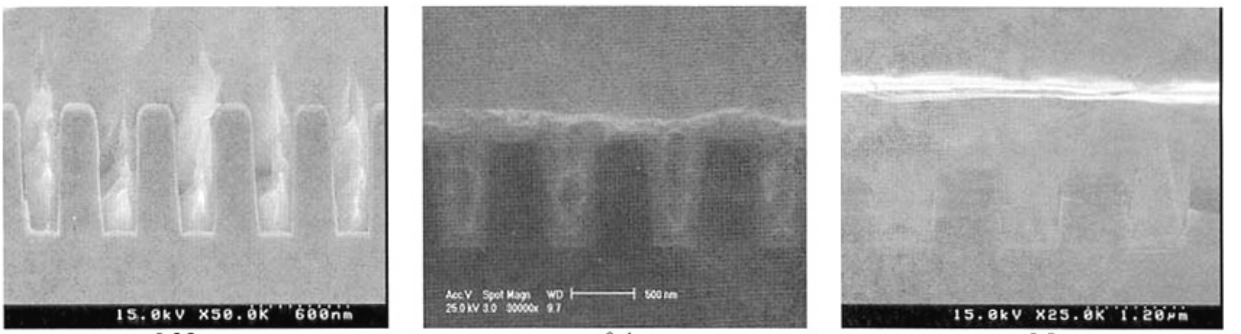
Fig. 2. FE-SEM cross-section view of electroplated trench with Pulse plating method at (a) 1A/ dm^2, (b) 3A / dm^2, (c) 7A/ dm^2.

(a) $1A/dm^2$



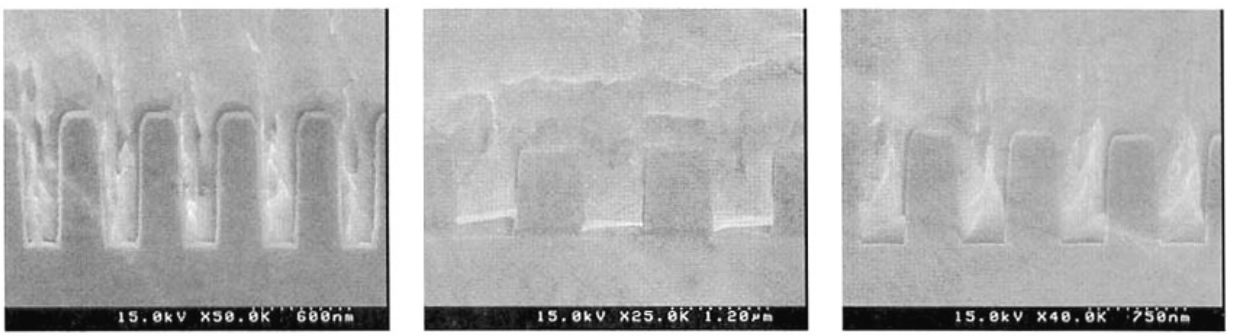
0.25㎛ 0.4㎛ 0.8㎛

(b) $3A/dm^2$



0.25㎛ 0.4㎛ 0.8㎛

(c) $7A/dm^2$



0.25㎛ 0.4㎛ 0.8㎛

Fig. 3. FE-SEM cross-section view of electroplated trench with DC plating method at (a) 1A/ dm^2 (b), $3A/dm^2$ (c), 7A/ dm^2.

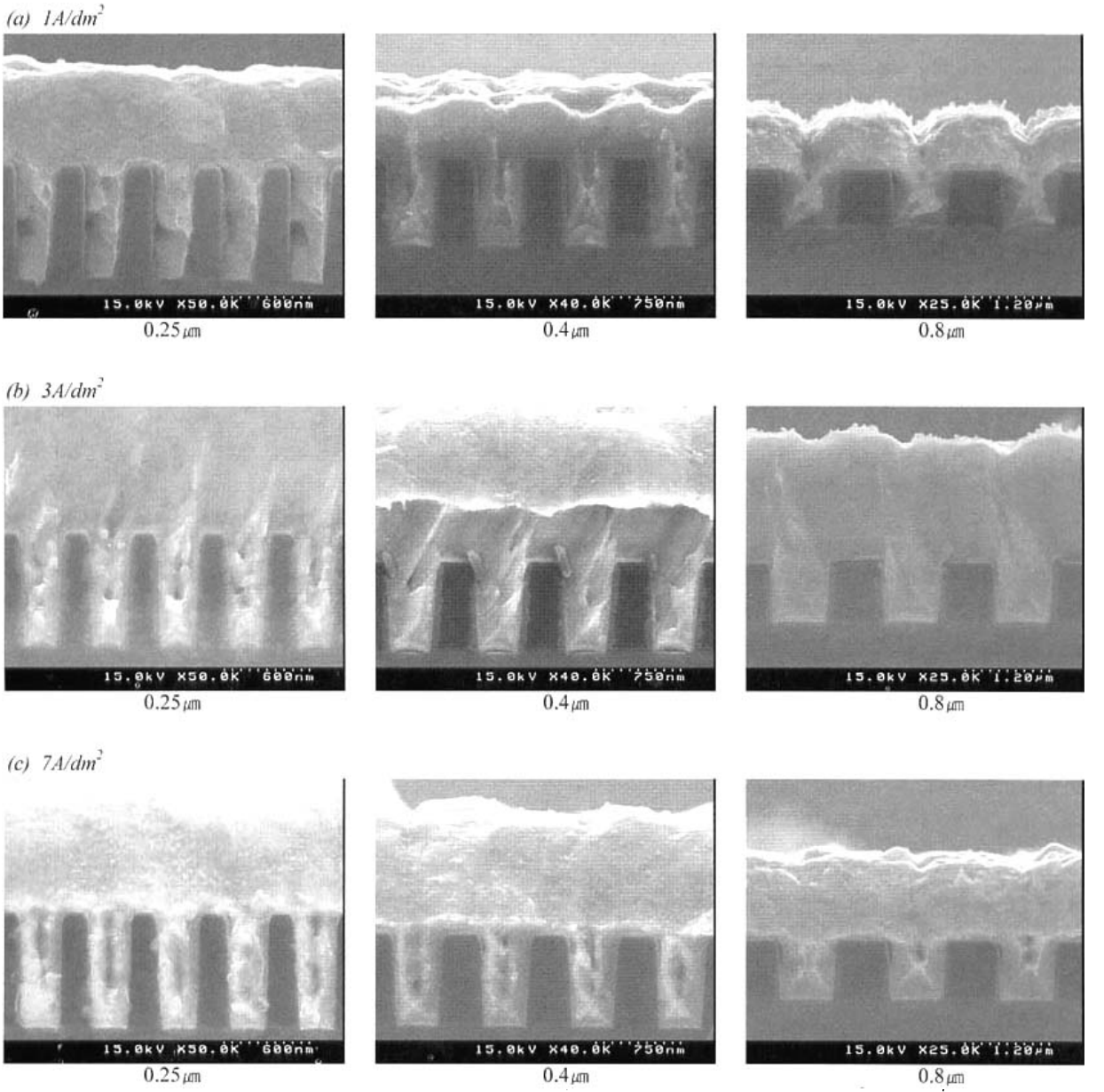


Fig. 4. FE-SEM cross-section view of electroplated trench with PR plating method at (a) 1A/dm^2, (b) 3A/ dm^2, (c) 7A/ dm^2

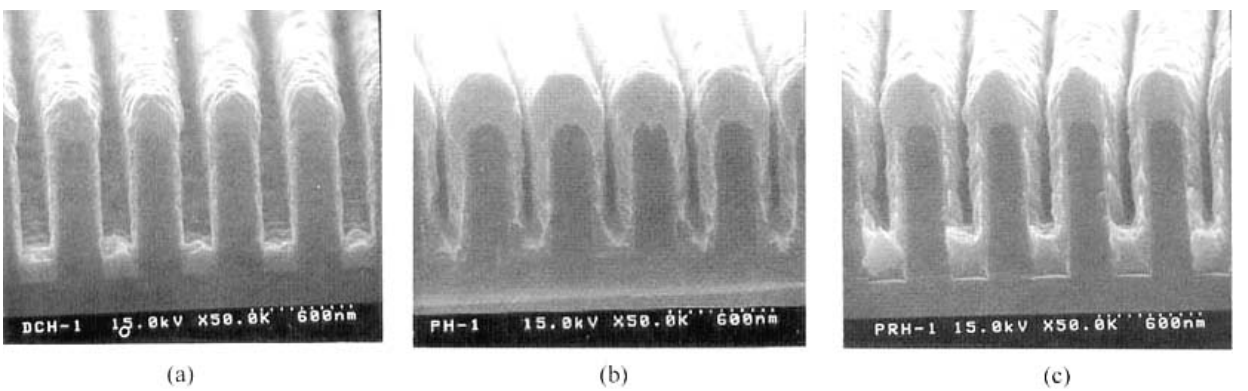


Fig. 5. FE-SEM cross-section view of unfinished trench fill ((a)DC (b) Pulse (c)PR plating).

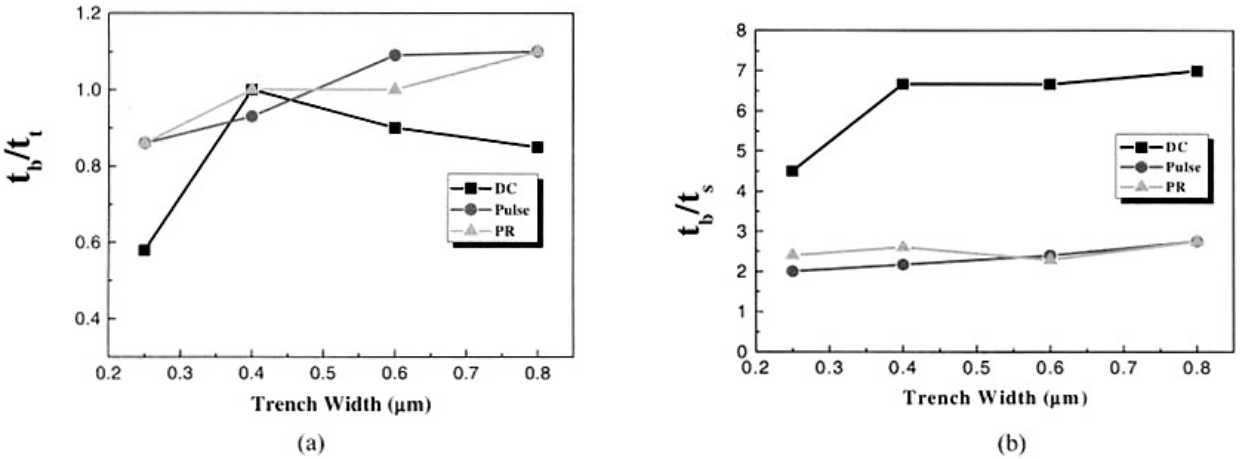


Fig. 6. The variation of aspect ratios with the trench width ((a)Bottom(t_b)/Top(t_t) thickness ratio (b)Bottom(t_b)/Side(t_s)/ thickness ratio).

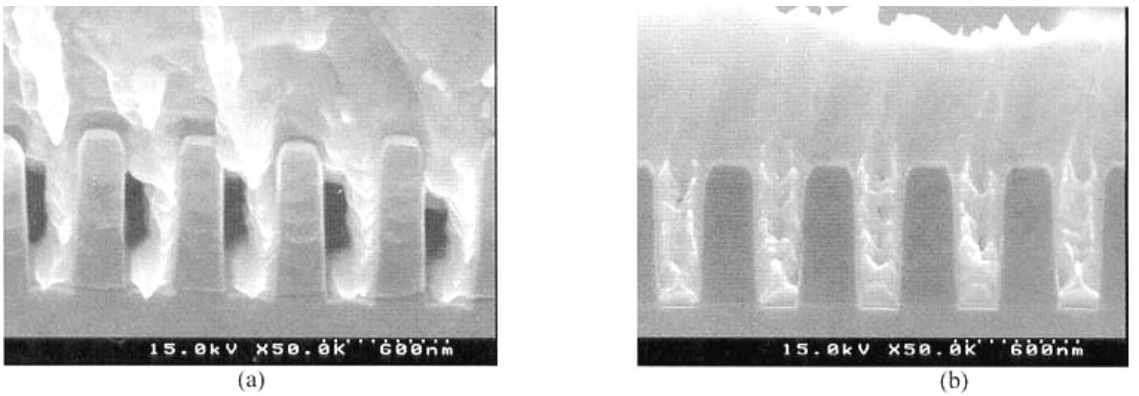


Fig. 7. FE-SEM views showing the filling characteristics of trench(0.25μm, 4 : 1 AR trench) (a)60s zero current induction time, (b)10s zero current induction time).

Cu dissolution during the pause and reverse current time intervals. PR plating, a corner and projecting parts were preferentially dissolved due to the higher current density, while for Pulse plating. Cu was also dissolved during pause time interval. Therefore Pulse or PR plating has less chance to have the entrance closure than DC plating has. Nevertheless center voids were observed even in the trenches electroplated by Pulse and PR. In order to understand this phenomenon, ratios of the bottom growth rate to the side growth rate were investigated in Figure 6(b). Pulse or PR plating have the higher ratio of the growth rate on the sidewall to the bottom than DC does. In Pulse and PR plating, the bottom growth rate is two times faster than the sidewall growth rate. In the case of center voids, DC plating may have the center voids in the final stage of plating due to the faster growth rate on the top than the bottom, while, PR and Pulse plating may have the center voids due to the faster plating rate on the sidewall.

Figure 7(a) shows the Sidewall void formed due to asymmetry seedlayer thickness. This is because seedlayer deposited by PVD has the poor coverage on the lower sidewall and bottom parts. In order to make wafer wet uniformaly, wafer is immersed in the plating-bath for a while before plating. According to Pourbaix diagram, both Cu2O and CuO oxides become unstable in a strongly acidic medium(pH < 3) due to their spontaneous decomposition with hydrogen ion, as follows.

$$Cu_2O + 2H^+ \rightarrow Cu^{2+} + Cu + H_2O$$
$$CuO + 2H^+ \rightarrow Cu^{2+} + H_2O$$

The too thin Cu seedlayer on one side may make nucleation difficult causing the void formation. In order to examine the cause of sidewall void formation, the wafers were electroplated with changing zero current induction time intervals.[7] Figure 8 shows cross-section images with 10s Figure 7(a) and 60s Figure 7(b) of zero

current induction time intervals. The longer zero current time interval, the easier sidewall void formation did. However sidewall void did not occur for the shorter zero current time interval. Therefore sidewall void formation is attributed to the localized corrosion of Cu seedlayer due to the long immersion of the wafer in the electrolyte before plating.

4. Conculusion

In this present work, Cu is electroplated with three types of current waveforms and various current densities on the wafer with trenches patterned silicon substrate. The cross-section images of the electroplated trench were observed by FE-SEM.

Trenches were successfully superfilled with Cu without void for Cu line with 0.4㎛ width irrespective of types of current waveforms. However voids were observed in Cu line with 0.25㎛ width. And current density values were optimized depending on types of wave forms.

The critical causes for the center and the sidewall void formations were investigated. Copper plating with DC current waveform may form the center void in final stage of plating because the growth velocity on the trench top corner was faster than that of inside of trench. On the contrary, Pulsed or PR current plating tends to form center voids due to the faster deposition on the sidewall. The sidewall void formation may result from the localized corrosion of copper seed layers due to the long immersion in the electrolyte before plating.

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